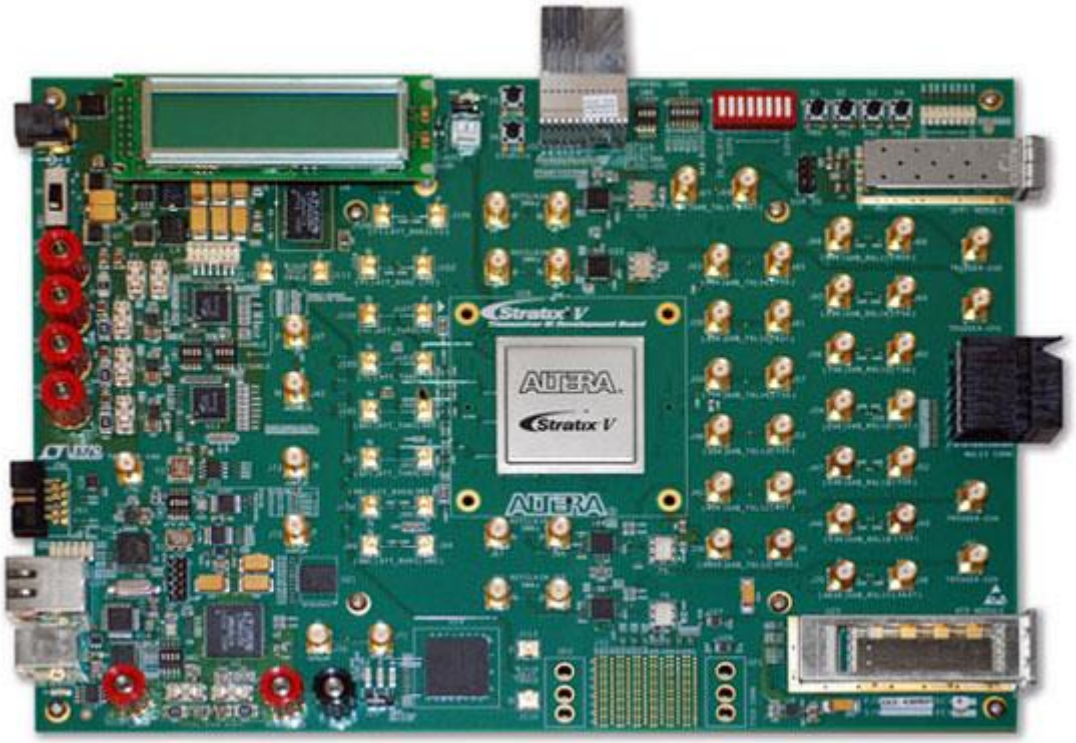
Altera Transceiver Signal Integrity Development Kit, Stratix V GX Edition

1. Overview



The Altera® Stratix® V GX Transceiver Signal Integrity (SI) Development Kit provides a platform for electrical compliance testing and interoperability analysis. The accessibility to multiple channels allows for real-world analysis as implemented in the system with transceiver channels available through SMA and popular backplane connectors. You can use this development kit to perform the following tasks:

- Evaluate transceiver link performance from 600 Mbps to 12.5 Gbps
- Generate and check pseudo-random binary sequence (PRBS) patterns via a simple to use GUI (does not require the Quartus® II software)
- Access advanced equalization to fine tune link settings for optimal bit error ratio (BER)
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to 10GbE, 10GBASE-KR, PCI Express® (PCIe®)(Gen1, Gen2, and Gen3), Serial RapidIO®, Gigabit Ethernet, 10-Gigabit Ethernet XAUI, Common Electrical I/O (CEI) 6G, CEI-11G, high-definition serial digital interface (HD-SDI), Interlaken, and other major standards

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- Use the built-in high speed backplane connectors to evaluate custom backplane performance and evaluate link BER

2. Specification

Featured device

- 5SGXEA7N2F40C2N

Configuration status and set-up elements

- JTAG
- On-board USB-Blaster™
- Fast passive parallel (FPP) configuration via MAX® II device and flash memory
- Two configuration file storage
- Temperature measurement circuitry (die and ambient temperature)

Clocks

- 50 MHz, 125 MHz, programmable oscillators (preset values: 624 MHz, 644.5 MHz, 706.25 MHz, and 875 MHz)
- SMA connectors for supplying an external differential clock to transceiver reference clock
- SMA connectors for supplying an external differential clock to the FPGA fabric
- SMA connectors to output a differential clock from the FPGA's phase-locked loop (PLL) output pin

General user input/output

- 10-/100-/1000-Mbps Ethernet PHY (RGMII) with RJ-45 (copper) connector
- 16x2 character LCD
- One 8-postion dipswitch
- Eight user LEDs
- Four user pushbuttons

Memory devices

- 128-megabyte (MB) sync flash memory (primarily to store FPGA configurations)

High speed serial interfaces

- Seven full-duplex transceiver channels routed to SMA connectors
    - Short trace routed on a micro-strip
    - Six strip-line channels from the with all the trace lengths are matched across channels

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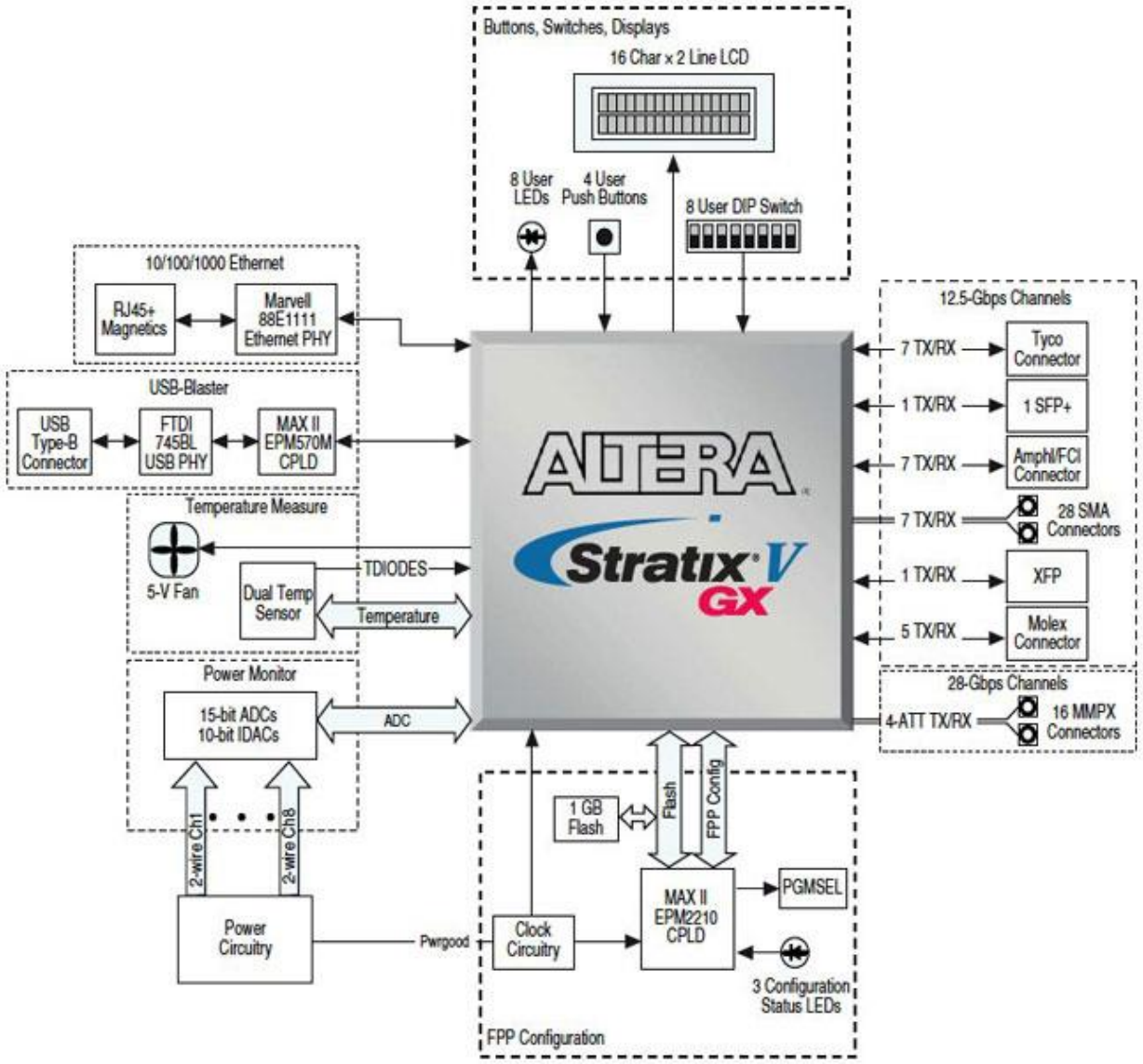
- 21 full-duplex transceiver channels routed to backplane connector
  - Seven channels to Molex® Impact® connector
  - Seven channels to Amphenol® XCede®
  - Seven channels to footprint of Tyco Strada® Whisper® (connector is not populated)

Power

- Laptop DC input
- Voltage margining

Stratix V GX Transceiver Signal Integrity Development Board Block Diagram



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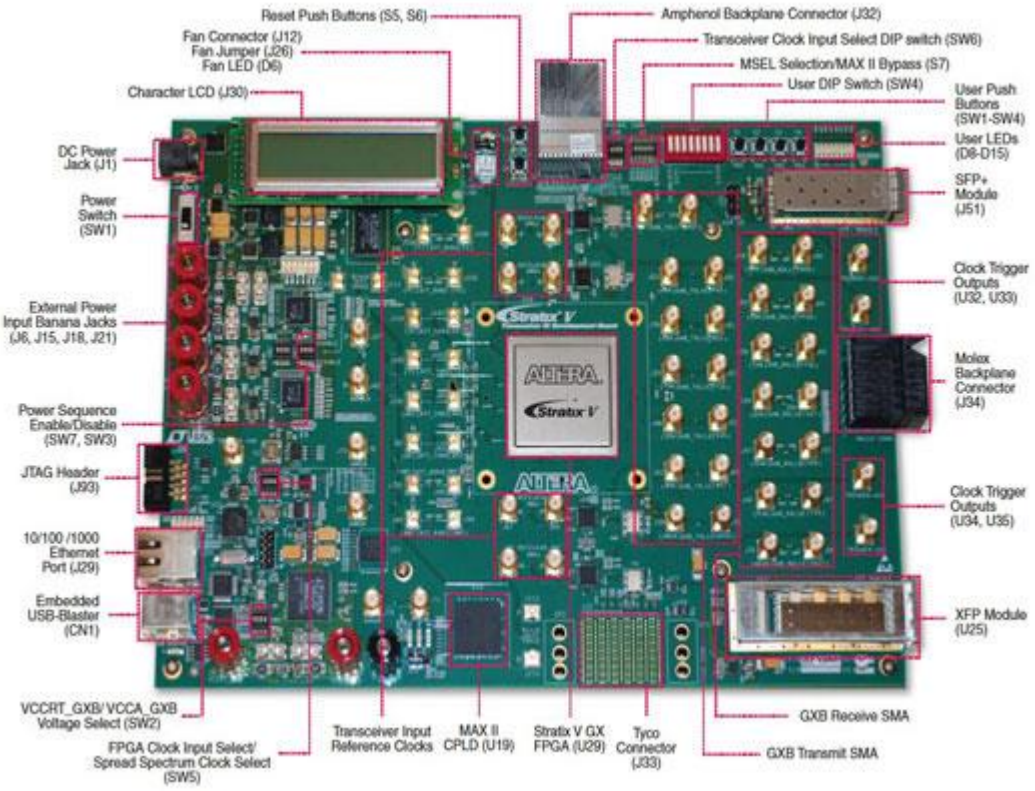
3. Kit content

- Altera's Complete Design Suite (download from Altera download center)
  - Quartus II software includes support for Stratix V FPGAs
  - 1-year license included
  - Nios® II Embedded Design Suite
  - MegaCore® intellectual property (IP) library includes PCIe, Triple-Speed Ethernet, Serial Digital Interface (SDI), and DDR3 SDRAM High-Performance Controller MegaCore IP cores
  - IP evaluation available through OpenCore Plus
- Board Update Portal
  - Featuring Nios II web server and remote system update
- GUI-based Board Test System
  - Interfaces to PC via JTAG
  - User controllable PMA settings (pre-emphasis, equalization, and so on)
  - Status indication (errors, BER, and so on)
- Complete documentation
- User guide
- Reference manual
- Board schematics and layout design file

4. Layout



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