Altera Stratix V Advanced Systems Development Kit

1. Overview

The Stratix® V Advanced Systems Development Kit is a complete systems design environment that includes both the hardware and software needed to begin architecture development and system design using Stratix V FPGAs. The PCI Express® (PCIe®)-based form-factor board combined with a one-year license for the Quartus® II software provide all that is needed to begin architecture development for a variety of applications. You can use this development kit to:

- Prototype and breadboard designs that take advantage of the widest bandwidth PCIe Gen3, x16 lane interfaces
- Develop and test memory subsystems consisting of DDR3, QDR II+, and MoSys® High Density serial interface memory
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to one of over 40 different HSMCs provided by Altera partners and supporting protocols such as Serial RapidIO® , 10-Gbps Ethernet (10GbE), SONET, Common Public Radio Interface (CPRI), OBSAI, and many others
- Utilize many third-party FMC modules to further expand connectivity to additional standard high-rate protocol modules like SFP+, QSFP, multi-rate SDI, DVB, and Ethernet AVB
- Combine all of these capabilities to prototype and demonstrate a full multi-FPGA complex processing system

2. Specification

Featured devices

- 5SGXEA7N2F45C2N = FPGA 1
- 5SGXEA7N2F45C2N = FPGA 2
- 5M2210ZF256C4N system controller

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- EPM570F100C5N on-board USB-Blaster™ II cable

External memory interfaces

- FPGA 1
  - 3072 MB 2x64+2x32 DDR3 SDRAM
  - 9 MB 2x18 QDRII+ SDRAM
  - 72 MB 4x72 MoSYS SRAM (10x10G XCVR)
  - 32 MB serial flash
- FPGA 2
  - 3072 MB 2x64+2x32 DDR3 SDRAM
  - 9 MB 2x18 QDRII+ SDRAM
  - 72 MB 4x72 MoSYS SRAM (10x10G XCVR)
  - 32 MB serial flash
- CPLD
  - 1 GB parallel flash for PFL

Clocks

- 50 MHz, 100 MHz, and 125 MHz programmable oscillators
- SMA input (LVDS)

General user input and output

- Each FPGA has 1 8-position dual in-line package (DIP) switch
- Each FPGA has 16 user LEDs
- Each FPGA has 3 user push buttons

Communication interfaces

- PCIe x16 edge connector to PLX PE8747 Gen3 Switch
  - One PCIe Gen3 x8 to each FPGA
- 1 FMC connector (FPGA 1)
- 1 HSMC port (FPGA 2)
- USB 2.0 on-board USB-Blaster II cable

Power

- Laptop DC input
- PCIe edge connector

Altera Stratix V Advanced Systems Development Board Block Diagram

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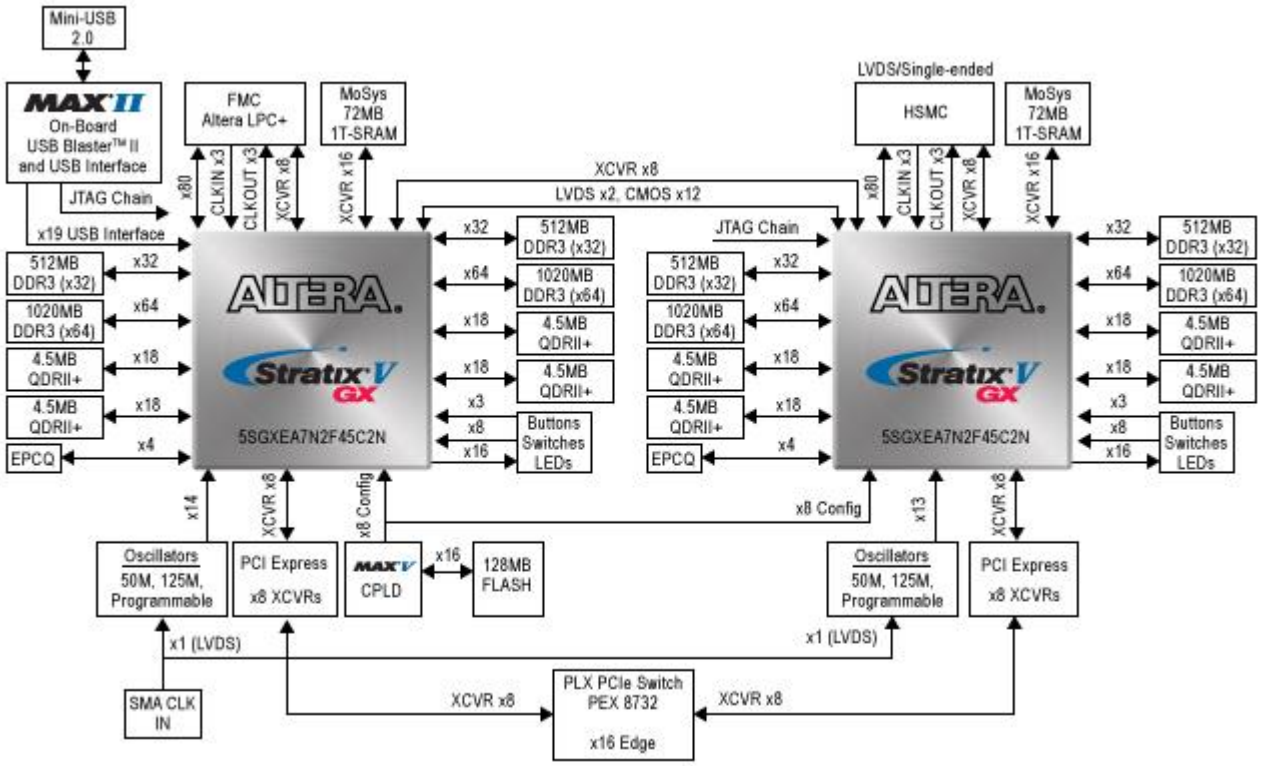

3. Kit content

- Power adapter and cables
- Stratix V Advanced Systems Development Kit software content
  - Complete documentation
    - User guide
    - Reference manual
    - Board schematics and layout design files
  - GUI-based Board Test System
    - Includes complete Quartus II projects with open source RTL
  - Quartus II design software, Development Kit Edition (DKE)
    - License to use full version of Quartus II software for one year

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